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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* ANDERS LANDIN and ERIK E. HAGERSTEN

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Appeal 2009-004059
Application 10/817,632[1]
Technology Center 2100

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Decided: January 11, 2010

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Before JOSEPH L. DIXON, JEAN R. HOMERE, and THU A. DANG, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Filed on April 2, 2004. This application claims priority from provisional application 60/460,580, which was filed on April 4, 2003. The real party in interest is Sun Microsystems, Inc. (App. Br. 2.)

## I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) (2002) from the Examiner's final rejection of claims 1 through 5, 7 through 14, and 16 through 20. (App. Br. 2.)[2] Claims 6 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. (*Id.*) We have jurisdiction under 35 U.S.C. § 6(b) (2008).

We affirm.

### *Appellants' Invention*

Appellants invented a method and system for performing coherent memory replication within multiprocessing computer systems. (Spec. 1, Para. [0001].) Appellants' Specification discloses that several different address spaces may be used to describe data stored in a computer system. (Spec. 10-11, Para. [0034].) Various translation functions may map an address specified in one address space to an address within another address space. (*Id.*) In particular, Appellants' Figure 6A depicts generating and transmitting virtual, global, and local physical addresses within various parts of computer system (100). (Spec. 20-21, Para. [0057].) According to Appellants, the claimed invention provides an improved system for implementing address translations between global and local physical addresses. (Spec. 3-4, Para. [0009].)

### *Illustrative Claim*

[2] All references to the Appeal Brief are to the Supplemental Appeal Brief filed on August 3, 2007, which replaced the prior Appeal Brief filed on May 21, 2007.

Independent claim 1 further illustrates the invention as follows:

1. A system, comprising:

a plurality of nodes, wherein each node includes an active device and a memory subsystem coupled to the active device;

wherein an active device in a node of the plurality of nodes is configured to generate a global address and translation information identifying a translation function, wherein the global address identifies a coherency unit;

wherein a memory subsystem included in the node is configured to select the translation function in response to the translation information and to perform the translation function on the global address to generate a physical address of the coherency unit within the memory subsystem;

wherein an additional memory subsystem included in an additional node of the plurality of nodes is configured to store the translation information identifying the translation function used in the node, wherein in response to a request for access to the coherency unit, the additional memory subsystem is configured to send the translation information to the node.

*Prior Art Relied Upon*

The Examiner relies on the following prior art as evidence of unpatentability:

| | | |
|---|---|---|
| Chi | 5,940,870 | Aug. 17, 1999 |
| Arimilli | 2002/0112124 A1 | Aug. 15, 2002 |
| Ang | 6,678,799 B2 | Jan. 13, 2004 (filed on Oct. 18, 2001) |

*Rejections on Appeal*

The Examiner rejects the claims on appeal as follows:

Claims 1 through 5, 7, 8, 10 through 14, and 16 through 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Chi and Ang.

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Chi, Ang, and Arimilli.

*Appellants' Contentions*

Appellants contend that Chi's disclosure of a node identification ("ID") and partition number does not teach any information that would identify a translation function. (App. Br. 5-7; 11-13.) Further, Appellants allege that Chi is only directed to a single translation function for all address translations and, therefore, does not teach selecting a translation function in response to translation information. (*Id.* at 7-8; 13-14.)

*Examiner's Findings and Conclusions*

The Examiner finds that Chi's disclosure translates the node ID and partition number of a global address to generate a physical address in each node and, therefore, teaches translation information identifying a translation function. (Ans. 9-11.) Further, the Examiner finds that Chi's disclosure of logic that utilizes an AMT Index in an address space to search an Address Mapping Table ("AMT") for a node ID corresponding to a global address teaches selecting different translation functions corresponding to different nodes. (*Id.*)

## II. ISSUE

Have Appellants shown that the Examiner erred in concluding that the combination of Chi and Ang renders independent claim 1 unpatentable? In particular, the issue turns on whether:

a) the proffered combination teaches "translation information identifying a translation function," as recited in independent claim 1;

b) the proffered combination teaches "select[ing] the translation function in response to the translation information," as recited in independent claim 1; and

c) the proffered combination teaches "stor[ing] the translation information identifying the translation function," as recited in independent claim 1.

## III. FINDINGS OF FACT

The following Findings of Fact ("FF") are shown by a preponderance of the evidence.

### *Chi*

1. Chi generally relates to distributed, shared-memory multiprocessor systems that employ a shared bus to connect multiple processors, memory modules, and input/output ("I/O") devices. (Col. 1, ll. 9-13.) Chi's Figure 8 depicts address translation from the source node to the destination node. (Col. 5, ll. 29-30.) The processor bus address (100) at the source node consists of two parts: an AMT Index (102) and an Offset (104). (*Id.* at ll. 30-32.) The AMT Index (102) is used to retrieve an entry from the AMT (106). (*Id.* at ll. 32-33.) Each table entry (108) contains a destination node ID for an access request on the processor bus. (*Id.* at ll. 33-35.) Note that the node ID from the AMT (106) is the physical node ID which is unique in the whole system. (*Id.* at ll. 43-45.) The partition number (110) is the logical ID within each application, such that there may be more than one application running on the system. (*Id.* at ll. 45-47.)

2. Chi discloses that the global address (112) on the interconnect is composed of the node ID (114) and the processor bus address (110) at the source node. (*Id.* at ll. 55-57.) This global address is part of the header of the packet sent from the source node to the destination node. (*Id.* at ll. 57-58.) At the destination node, the node ID is stripped off and the partition number is replaced with 0, such that the translated address (116) falls in the local space of the destination node. (*Id.* at ll. 58-61.) Finally, the private memory size (118) at the destination node (or the starting address of the near global memory of the destination node) is further added to produce the processor bus address (120) to be used at the destination node. (*Id.* at ll. 62-65.)

## IV. PRINCIPLES OF LAW

### *Obviousness*

"On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness." *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998) (citations omitted).

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," and discussed circumstances in which a patent might be determined to

be obvious. *Id.* at 415 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)). The Court reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* at 416. The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 415, 417.

In identifying a reason that would have prompted a person of ordinary skill in the relevant field to combine the prior art teachings, the Examiner must show "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

## V. ANALYSIS

### *Claim 1*

Independent claim 1 recites, in relevant part:

> 1) "translation information identifying a translation function;" 2) "select[ing] the translation function in response to the translation information;" and 3) "stor[ing] the translation information identifying the translation function."

As detailed above in the Findings of Fact section, Chi discloses translating an address from a source node to a destination node. (FF 1.) In particular, Chi's disclosure indicates retrieving an entry containing a destination node ID from an AMT utilizing the AMT Index of a corresponding address space. (*Id.*) We find that Chi's disclosure of an AMT Index that corresponds to a destination node ID in an AMT teaches translation information that identifies a translation function. We also find

that an ordinarily skilled artisan would have readily appreciated that utilizing an AMT Index to select a corresponding destination node ID in an AMT amounts to selecting a translation function in response to translation information. Thus, we find that Chi's cited disclosure teaches "translation information identifying a translation function" and "select[ing] the translation function in response to the translation information," as recited in independent claim 1.

Further, Chi discloses that the global address consists of a node ID and a processor bus address at the source node. (FF 2.) The global address is part of a packet header sent from the source node to the destination node. (*Id.*) At the destination node, the node ID is stripped off and the partition number is replaced with 0, whereby the corresponding translated address is stored in the local space of the destination node. (*Id.*) We find that Chi's disclosure of stripping the node ID off the global address and replacing the partition number with 0 at the destination node teaches performing a different translation function on the global address at an additional node. We also find that Chi's disclosure of storing the translated address in the local space on the destination node teaches storing translation information identifying a translation function at an additional node. Thus, we find that Chi's cited disclosure teaches "stor[ing] the translation information identifying a translation function," as recited in independent claim 1. It follows that Appellants have not shown that the Examiner erred in concluding that the combination of Chi and Ang renders independent claim 1 unpatentable.

*Claims 2, 4, 5, 7, 8 through 10, 11, 13, 14, and 16 through 20*

Appellants do not provide separate arguments with respect to claims 2, 4, 5, 7, 8 through 10, 11, 13, 14, and 16 through 20. Therefore, we select independent claim 1 as representative of the cited claims in this grouping. Consequently, Appellants have not shown error in the Examiner's rejection claims 2, 4, 5, 7, 8 through 10, 11, 13, 14, and 16 through 20 for the reasons set forth in our discussion of independent claim 1. 37 C.F.R. § 41.37(c)(1)(vii).

*Claims 3 and 12*

Appellants contend that Chi is only directed to a single translation function for all address translations and, therefore, does not teach that "the additional memory subsystem is configured to perform a different translation function on the global address," as recited in dependent claim 3. (App. Br. 8-9.) We do not agree.

As set forth above, we find that Chi's disclosure of stripping the node ID off the global address and replacing the partition number with 0 at the destination node teaches performing a different translation function on the global address at an additional node. Thus, we find the Chi's cited disclosure teaches the disputed limitation. It follows that Appellants have not shown that the Examiner erred in concluding that the combination of Chi and Ang renders dependent claim 3 unpatentable.

Appellants do not provide separate arguments with respect to dependent claim 12. Therefore, we select dependent claim 3 as representative of the cited claim. Consequently, Appellants have not shown error in the Examiner's rejection dependent claim 12 for the reasons set forth in our discussion of dependent claim 3. 37 C.F.R. § 41.37(c)(1)(vii).

## VI. CONCLUSION OF LAW

Appellants have not shown that the Examiner erred in rejecting claims 1 through 5, 7 through 14, and 16 through 20 as being unpatentable under 35 U.S.C. § 103(a).

## VII. DECISION

We affirm the Examiner's decision to reject claims 1 through 5, 7 through 14, and 16 through 20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(iv).

AFFIRMED

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